1W Fully Differential Audio Power Amplifier with Internal Feedback Resistors

CE0030B

■ INTRODUCTION

The CE0030B is a fully differential audio power amplifier designed for portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from 5V battery voltage. It operates from 2.2 to 6.8V. Features like 83dB PSRR at 217Hz, improved RF-rectification immunity, the space-saving 8-pin MSOP8 and SOP8 package, the advanced pop & click circuitry, a minimal count of external components and low-power shutdown mode make CE0030B ideal for wireless handsets. The CE0030B is unity-gain stable, and the gain can be configured by external input resistors and internal feedback resistors.

■ FEATURES

- Fully differential amplifier
- Improved PSRR at 217Hz（V_{DD}>3.0V）83dB (Typ.)
- Power output at 5.0V & 1% THD 1W (Typ.)
- Power output at 3.6V & 1% THD 0.5W (Typ.)
- Ultra low shutdown current 0.1μA (Typ.)
- Improved pop & click circuitry eliminates noises during turn-on and turn-off transitions
- Thermal overload protection circuitry
- No output coupling capacitors, bootstrap capacitors required
- Unity-gain stable
- External gain configuration capability
- Available in space-saving packages: 8-pin MSOP8, SOP8, DIP8 & DICE

■ APPLICATIONS

- Wireless handsets
- Portable audio devices
- PDAs,
- Notebook computer

■ ORDER INFORMATION

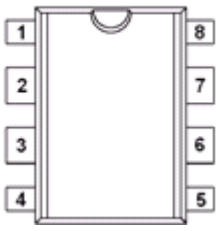
CE0030B①

DESIGNATOR	SYMBOL	DESCRIPITION
①	SM	Package: MSOP8
	S	Package: SOP8
	D	Package: DIP8
	—	Package: DICE

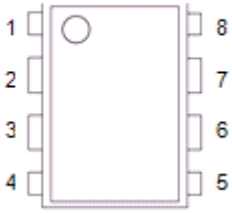
■ PIN DIAGRAM

MSOP-8 Package

SOP-8 Package



DIP-8 Package



■ PIN CONFIGURATION

MSOP8	SOP8	DIP8	SYMBOL	TYPE	FUNCTION
1	1	1	SPN	O	Negative output.
2	2	2	SPP	O	Positive output.
3	3	3	V_{SS}	I	Ground.
4	4	4	INN	I	Negative input.
5	5	5	ACIN	I	Positive input.
6	6	6	VREF	O	Common-mode voltage，connect a Bypass capacitor to Ground.
7	7	7	CE	I	Chip Enable Logical Control, “High” is active.
8	8	8	V_{DD}	O	Power Supply.

■ BLOCK DIAGRAM AND TYPICAL APPLICATION

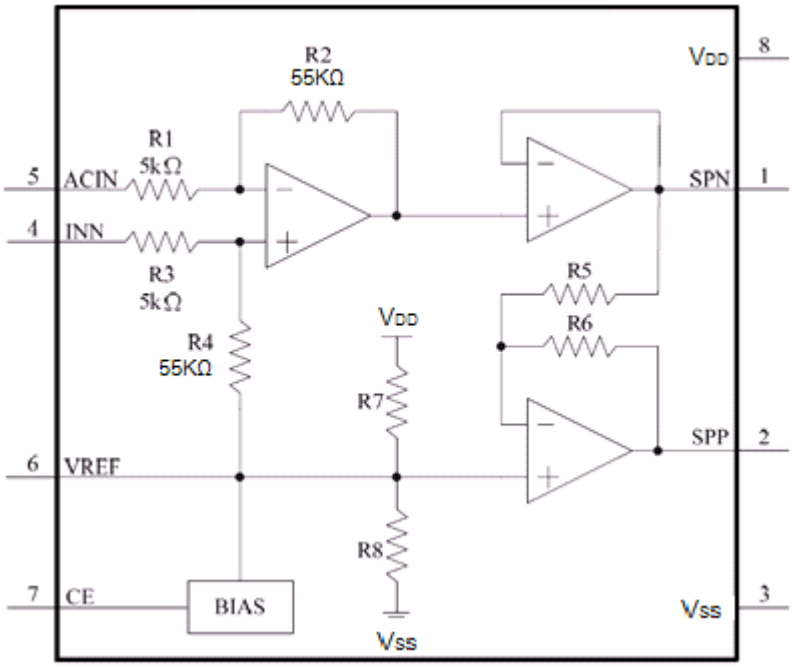


Fig1 BLOCK DIAGRAM

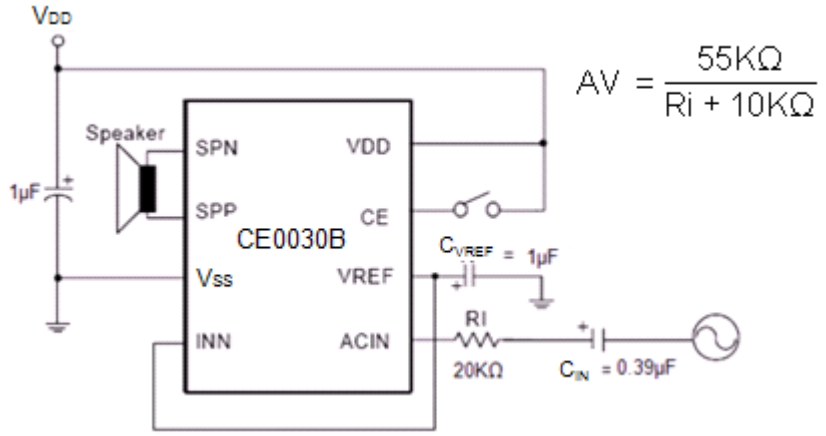


Fig2 SINGLE END APPLICATION

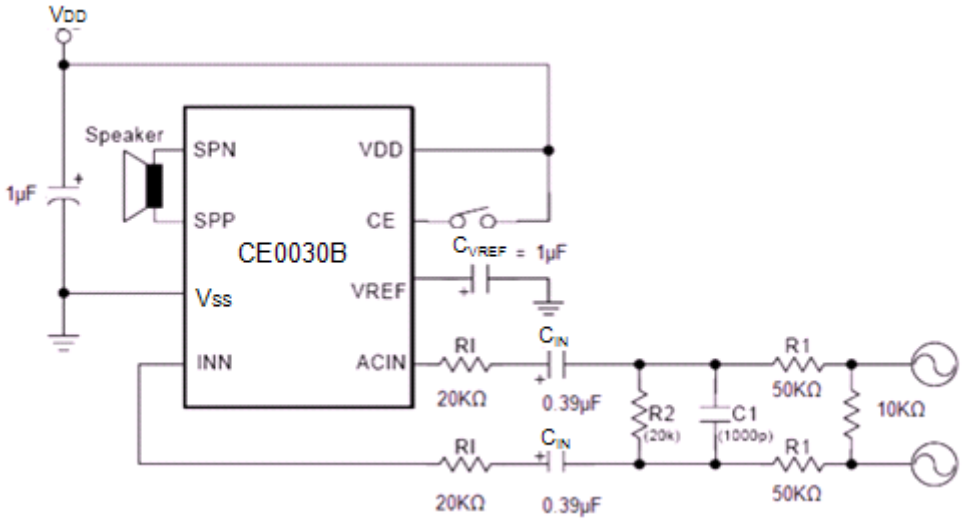


Fig3 DOUBLE END APPLICATION (With Input Filter Circuit)

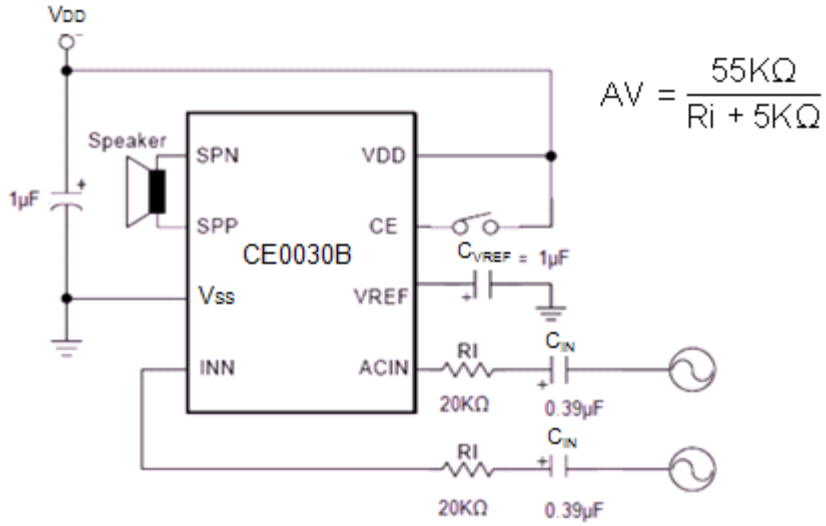


Fig4 DOUBLE END APPLICATION (Without Input Filter Circuit)

Note： Capacitor in the application can be Tantalum, Electrolytic and Ceramic etc.

■ ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, Ta=25°C)

PARAMETER		SYMBOL	RATINGS	UNITS
V_{DD} pin voltage		V_{DD}	$V_{SS}-0.3 \sim V_{SS}+8$	V
Power dissipation	MSOP8	PD	500	mW
	SOP8	PD	300	mW
	DIP8	PD	500	mW
Operating temperature		T_{opr}	−40 ~+85	°C
Storage temperature		T_{stg}	−40 ~+125	°C
Soldering Temperature & Time		T_{solder}	260℃, 10s	

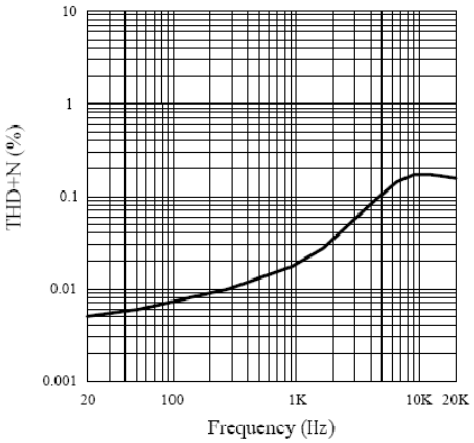
■ ELECTRICAL CHARACTERISTICS

V_{DD}＝5V(8Ω load，AV＝1V，Ta＝25℃)

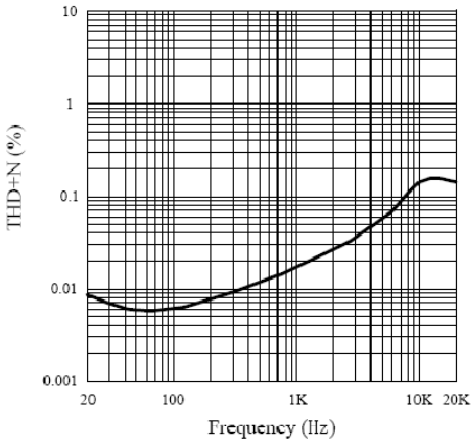
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operation Voltage	V_{DD}		2.2		6.8	V
Current consumption	I_{DD}	V_{DD} =5V,V_{CE}＝V_{DD}，No Load		2.5		mA
		V_{DD} =5V,V_{CE}＝V_{DD}，R_L＝8Ω		4		mA
Current consumption during shutdown	I_{SHDN}	Shutdown＝V_{SS}		0.1	1.0	μA
Output Power	P_O	THD＝1％（max）；f＝1KHz		1		W
Total Harmonic Distortion Noise	THD+N	Po=0.6Wrms；f=1KHz		0.1		%
Power Supply Rejection Ratio	PSRR	V_{ripple}＝200mV sine P-P				
		f＝217Hz		-83		dB
		f＝1KHz		-83		dB
Common Mode Rejection Ratio	CMRR	f=217Hz，V_{CM}＝200mV_{pp}		-78		dB
Output Offset Voltage	V_{OS}	V_{IN}＝0V		2		mV
Shutdown Voltage Input High	V_{SDIH}		1.5			V
Shutdown Voltage Output Low	V_{SDIL}				0.3	V
Closed Loop Gain	A_V		$\frac{50K\Omega}{Ri+5K\Omega}$	$\frac{55K\Omega}{Ri+5K\Omega}$	$\frac{60K\Omega}{Ri+5K\Omega}$	V/V
Enable Time	T_{ON}	V_{DD}=5V,C_{IN}=0.39μF, C_{VREF}=0.33μF		50		ms
		V_{DD}=3V,CIN=0.39μF, C_{VREF}=0.33μF		35		ms

■ TYPICAL PERFORMANCE CHARACTERISTICS

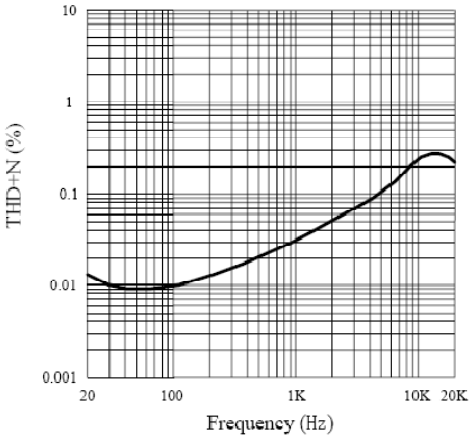
THD+N vs Frequency
V_{DD}=5V, R_L=8 Ω ,P_O=600mW



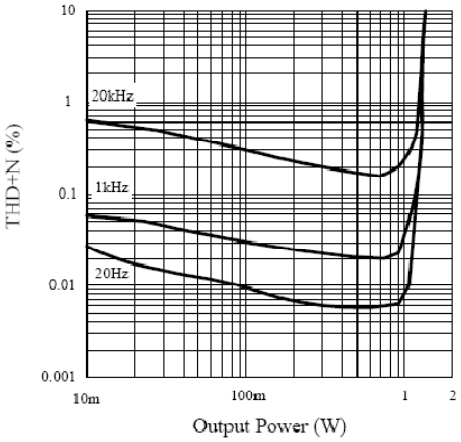
THD+N vs Frequency
V_{DD}=3.6V, R_L=8 Ω ,P_O=400mW



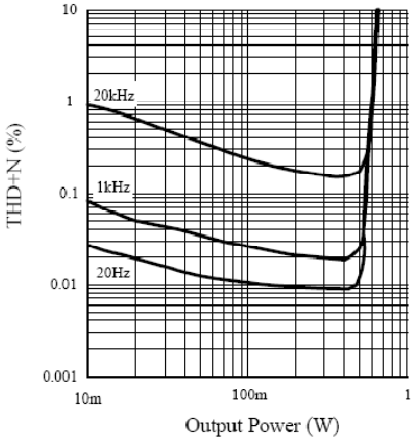
THD+N vs Frequency
V_{DD}=2.5V, R_L=8 Ω ,P_O=150mW



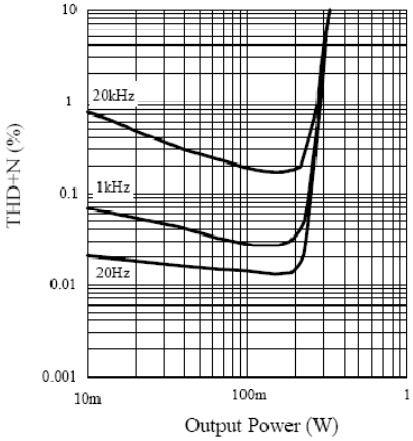
THD+N vs Output Power
V_{DD}=5V, R_L=8 Ω



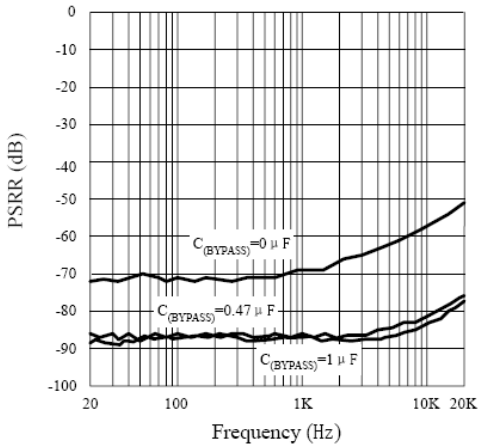
THD+N vs Output Power
V_{DD}=3.6V, R_L=8 Ω



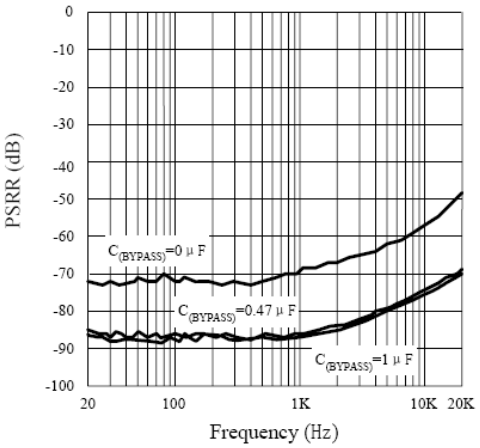
THD+N vs Output Power
V_{DD}=2.5V, R_L=8 Ω



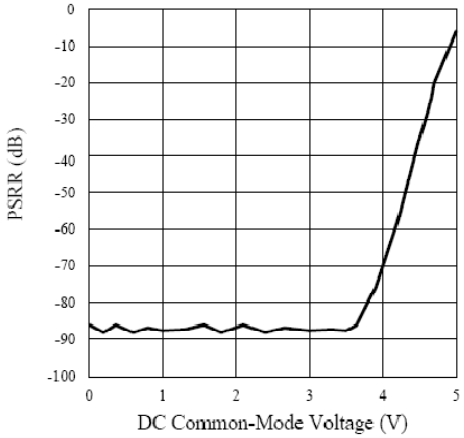
PSRR vs Frequency
V_{DD}=5.0V, R_L=8Ω ,input 10Ω Terminated



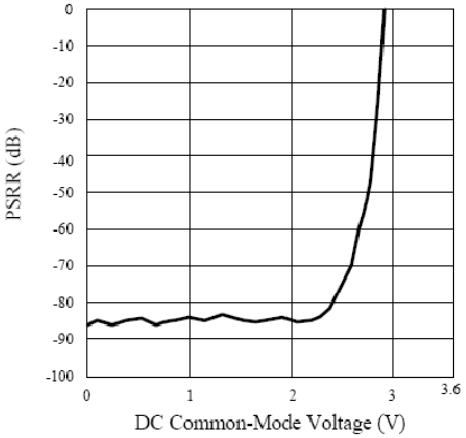
PSRR vs Frequency
V_{DD}=3.6V, R_L=8Ω ,input 10Ω Terminated



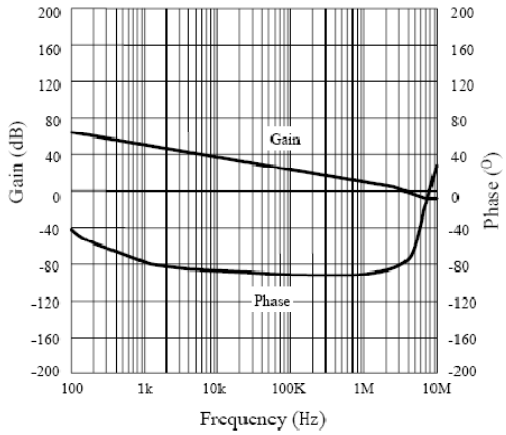
PSRR vs Common Mode voltage
V_{DD}=5.0V, R_L=8Ω , 217Hz, 200mV_{PP}



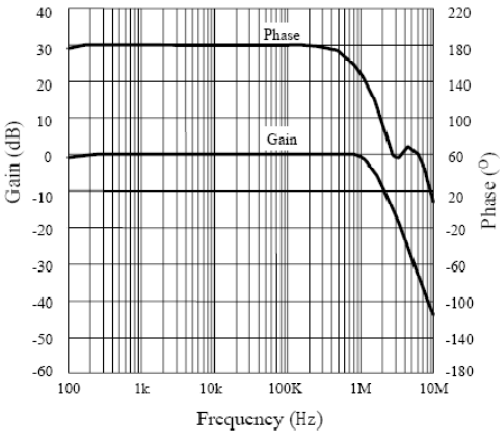
PSRR vs Common Mode voltage
V_{DD}=3.6V, R_L=8Ω , 217Hz, 200mV_{PP}



Open Loop Frequency Response

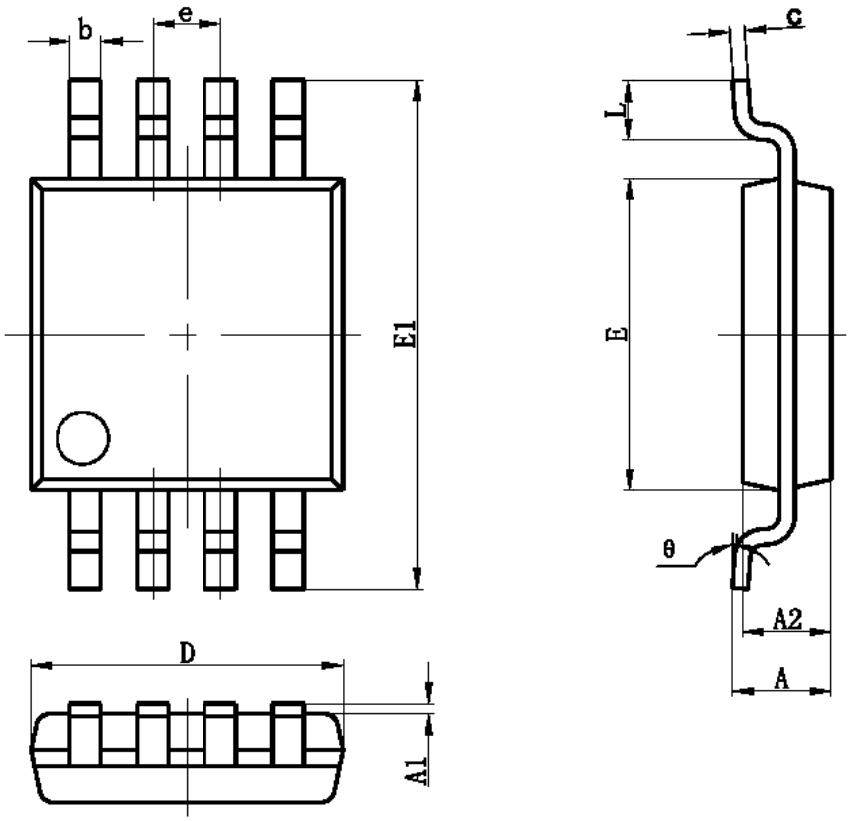


Closed Loop Frequency Response



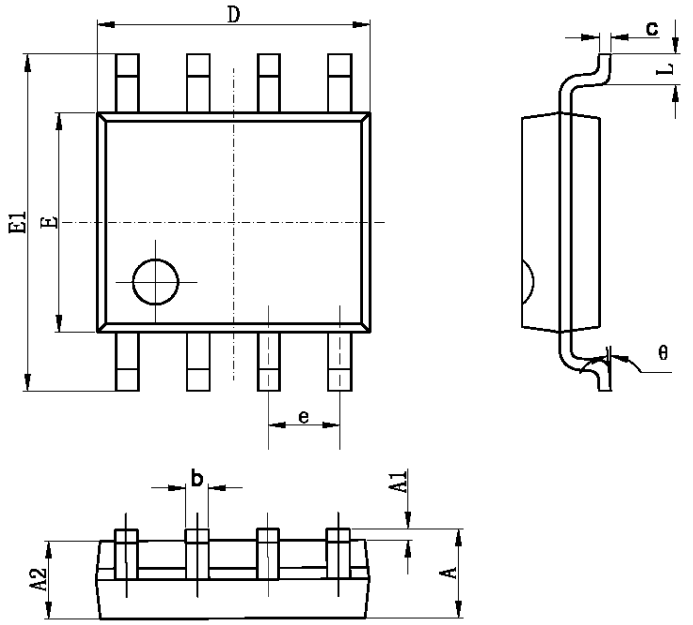
■ PACKAGING INFORMATION

● MSOP8 PACKAGE OUTLINE DIMENSIONS



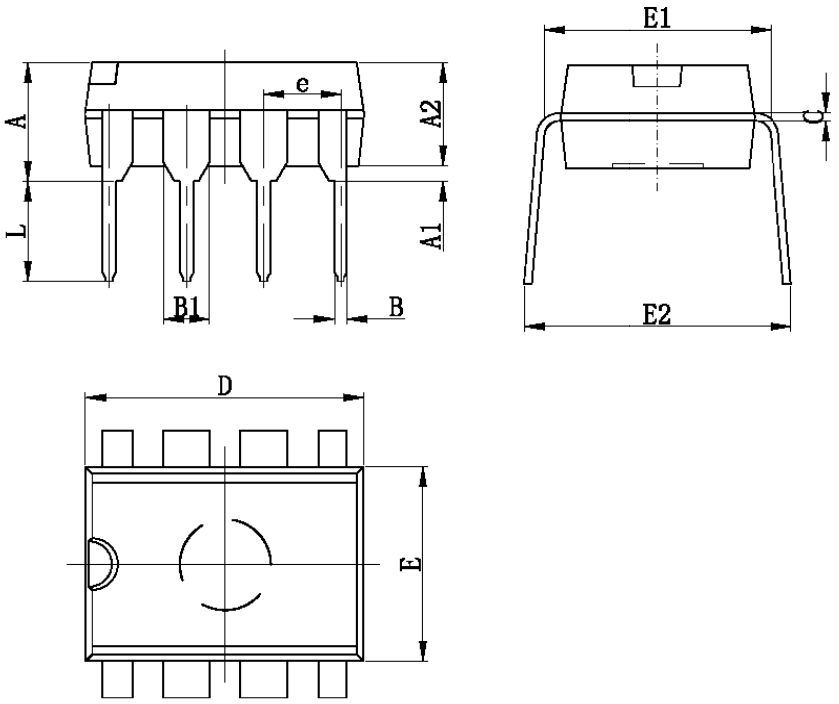
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

- **SOP8 PACKAGE OUTLINE DIMENSIONS**



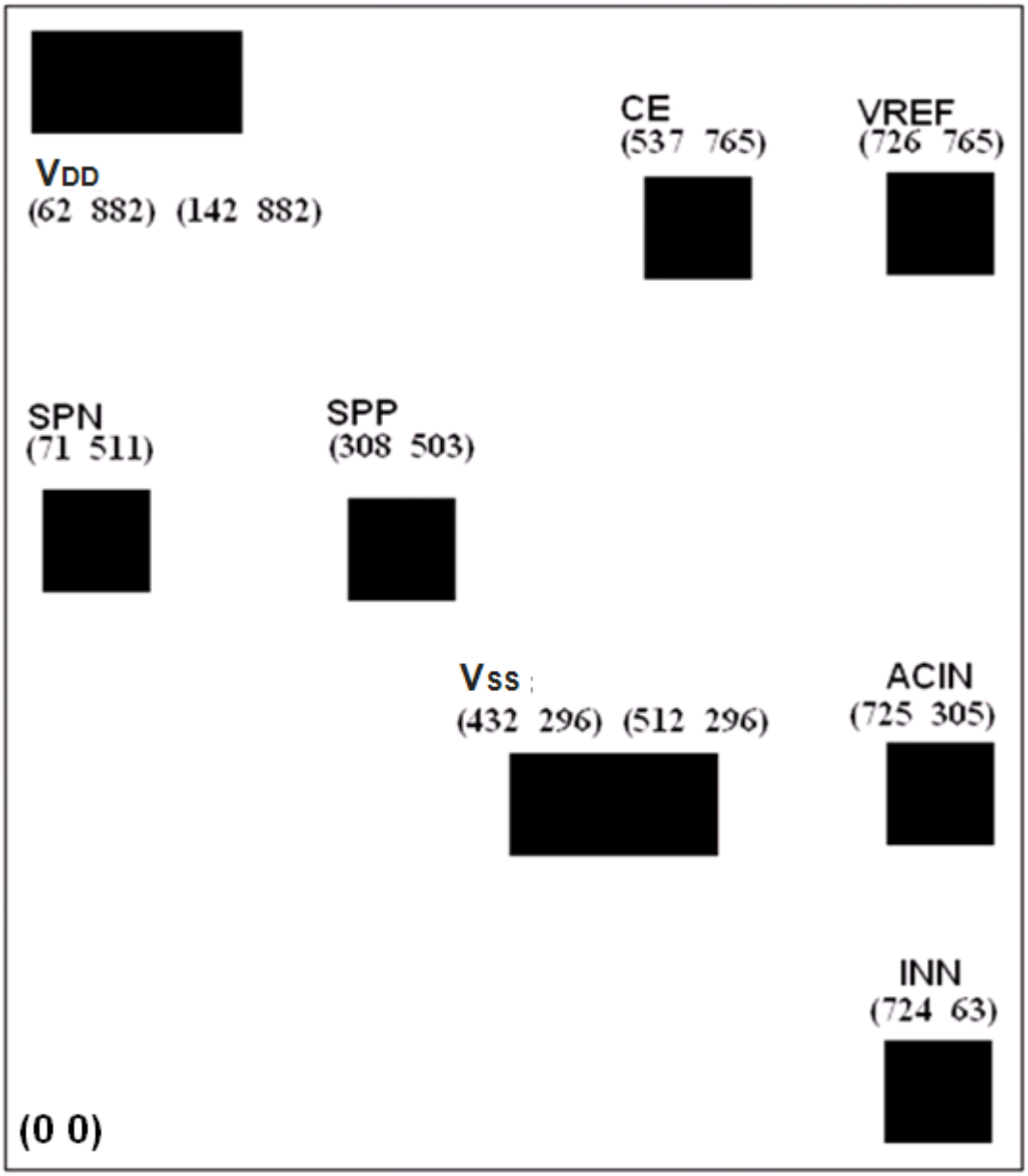
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

- **DIP8 PACKAGE OUTLINE DIMENSIONS**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

■ PAD ASSIGNMENT



This IC substrate should be connected to V_{SS}